WHAT IS CLAIMED IS:

1. A processor comprising:

a replay system to replay instructions which have not executed properly;

a first processing circuit coupled to the replay system to process instructions including any replayed instructions;

a second processing circuit to perform additional processing on an instruction, the second processing circuit having an ability to detect one or more faults occurring therein; and

a synchronization circuit coupled between the first processing circuit and the second processing circuit to synchronize faults occurring in the second processing circuit to matching instruction entries in the first processing circuit.

2. The processor of claim 1 wherein the first processing circuit comprises a first event pipeline, and wherein the second processing circuit comprises a second event pipeline.

3. A method comprising:

detecting that an instruction has not executed properly;

replaying an instruction in a first event pipeline;

performing additional processing on an instruction in a second event pipeline;

detecting a fault for the instruction occurring in the second event pipeline;

matching the instruction having a fault which occurred in the second event pipeline to an instruction entry for the same instruction that is being replayed in the first event pipeline;

writing or tagging fault identification information for the fault to the matching instruction entry in the first event pipeline.

4. A processor comprising:

a replay system to replay instructions which have not executed properly;

a synchronous event pipeline coupled to the replay system to process instructions including any replayed instructions;

an asynchronous event pipeline to perform additional processing on an instruction, the asynchronous event pipeline having an ability to detect one or more asynchronous faults occurring during the additional instruction processing; and

a synchronization circuit coupled between the synchronous event pipeline and the asynchronous event pipeline to synchronize an asynchronous fault with a replayed instruction in the synchronous event pipeline.

5. The processor of claim 4 wherein the synchronization circuit comprises:

a buffer coupled to the asynchronous event pipeline for storing an instruction entry for an instruction having an asynchronous fault, the instruction entry including a sequence number and fault identification information identifying the asynchronous fault; and

a comparator coupled to the buffer and the synchronous event pipeline, the comparator comparing a sequence number of an instruction entry in the synchronous event pipeline with the sequence number of the instruction entry having the asynchronous fault, and writing the fault

identification information of the asynchronous fault to the instruction entry in the synchronous event pipeline if a match is found.

6. The processor of claim 4 wherein the synchronization circuit comprises:

an input buffer coupled to the asynchronous event pipeline for storing an instruction entry for an instruction having an asynchronous fault, the instruction entry including a sequence number and fault identification information identifying the asynchronous fault;

an asynchronous fault buffer having age guarding logic coupled to the input buffer, the asynchronous fault buffer storing an instruction entry for an instruction having an asynchronous fault in a temporary register; and

a comparator coupled to the asynchronous fault buffer and the synchronous event pipeline, the comparator comparing a sequence number of an instruction entry in the synchronous event pipeline with a sequence number of the instruction entry stored in the temporary register of the asynchronous fault buffer, and writing the fault identification information of the asynchronous fault to the instruction entry in the synchronous event pipeline if a match is found.

7. The processor of claim 6 wherein the asynchronous fault buffer comprises:

age guarding logic coupled to the input buffer; and

a temporary register coupled to the age guarding logic to store an instruction entry for an instruction having an asynchronous fault, the age guarding logic maintaining an oldest instruction entry in the register as compared between an instruction entry having an asynchronous fault already

present in the temporary register and an instruction entry for an instruction having an asynchronous fault stored in the input buffer.

8. The processor of claim 6 wherein the asynchronous fault buffer comprises:

age guarding logic coupled to the input buffer;

one or more temporary registers coupled to the age guarding logic to store one or more oldest instruction entries for an instruction having an asynchronous fault, the age guarding logic maintaining an oldest instruction entry in each temporary register as compared between an instruction entry having an asynchronous fault already present in the temporary register and an instruction entry for an instruction having an asynchronous fault stored in the input buffer; and

a mux coupled to the one or more temporary registers for selectively outputting the instruction entry from a selected temporary register to the comparator.

9. The processor of claim 8 wherein there is one temporary register provided for each thread or program flow.

10. A processor comprising:

a replay system to replay instructions which have not executed properly;

a memory execution unit coupled to the replay system to execute load and store instructions, the memory execution unit including:

a synchronous event pipeline to execute load or store instructions, including instructions which have been replayed;

an asynchronous event pipeline coupled to the synchronous event pipeline for performing additional processing on instructions, the asynchronous event pipeline having an ability to detect one or more asynchronous faults occurring during the additional instruction processing in the asynchronous event pipeline; and

a synchronization circuit coupled between the synchronous event pipeline and the asynchronous event pipeline to synchronize an asynchronous fault with a replayed instruction in the synchronous event pipeline.

11. The processor of claim 10 wherein said synchronization circuit comprises a comparator circuit to compare a sequence number of an instruction entry in the asynchronous event pipeline having a fault to sequence numbers of instruction entries in the synchronous pipeline, the comparator circuit writing fault identification information identifying the asynchronous fault to the instruction entry in the synchronous event pipeline if a match is found.

12. A processor comprising:

a replay system to replay instructions which have not executed properly;

a plurality of synchronous event pipelines coupled to the replay system to process instructions including any replayed instructions;

an asynchronous event pipeline to perform additional processing on an instruction, the asynchronous event pipeline having an ability to detect one or more asynchronous faults occurring during the additional instruction processing in the asynchronous event pipeline;

a synchronization circuit coupled between the synchronous event pipeline and the asynchronous event pipeline to synchronize an asynchronous fault with a replayed instruction in the synchronous event pipeline;

a fault register; and

age guarding logic coupled between the plurality of synchronous event pipelines and the fault register, the age guarding logic storing fault information in the fault register for an oldest instruction entry as compared between the instruction entries from the plurality of synchronous pipelines and the fault information already present in the fault register.

13. The processor of claim 12 wherein the fault register stores fault information for an oldest instruction entry, the fault information including a specific fault code and an address.

14. A method of processing faults in a processor comprising:

detecting that an instruction has executed improperly;

replaying the instruction;

performing additional processing on the instruction;

detecting a fault in the additional instruction processing;

writing fault identification information to an instruction entry for the replayed instruction.

15. The method of claim 14 wherein the writing fault identification information comprises:

comparing a sequence number of the instruction entry for the replayed instruction with the sequence number of the instruction having the fault;

writing fault identification information to the instruction entry for the replayed instruction if there is a match.

16. The method of claim 14 wherein said performing additional processing comprises performing a long latency operation for the instruction in parallel with the instruction being replayed.

17. A method comprising:

detecting that an instruction has executed improperly;

replaying the instruction in a synchronous event pipeline;

performing additional processing on the instruction in an asynchronous event pipeline;

detecting an occurrence of an asynchronous fault during the additional processing of the instruction in the asynchronous event pipeline;

identifying that the instruction in the asynchronous event pipeline having the fault matches the replayed instruction in the synchronous event pipeline; and

writing fault identification information into an instruction entry for the replayed instruction in the synchronous event pipeline.

18. The method of claim 17 wherein said replaying comprises replaying the instruction in one of a plurality of synchronous event pipelines.

19. The method of claim 17 and further comprising storing fault identification information for an oldest instruction in a fault register as compared between the instruction entry in the synchronous event pipeline having the fault identification information and fault identification information already present in the fault register.

20. An apparatus comprising:

a replay system to replay instructions which have not executed properly;

a first event pipeline;

a second event pipeline, the processor detecting a fault for an instruction in the second event pipeline;

a circuit coupled to the first and second event pipelines to add a fault identifier identifying the fault occurring in the second event pipeline to a corresponding instruction entry in the first event pipeline when the instruction is replayed.

21. An apparatus comprising:

a replay system to replay instructions which have not executed properly;

an age guarding circuit to add a fault identifier to an instruction entry for an instruction that is being replayed.

22. The apparatus of claim 21 wherein the age guarding circuit adds a fault identifier for an asynchronous or long latency fault occurring in an asynchronous event pipeline to a corresponding instruction entry in a synchronous or short latency event pipeline.